

AD7590DI/AD7591DI/AD7592DI

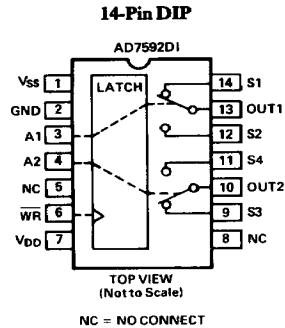
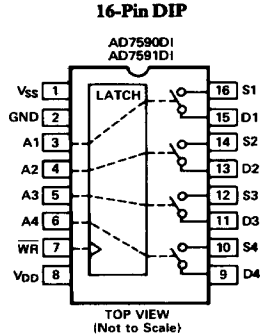
FEATURES

SCR Latch-Proof
Overvoltage-Proof: $\pm 25V$
Low R_{ON} : 60Ω typ
Buffered Switch Logic
TTL, CMOS Compatible
Monolithic Dielectrically-Isolated CMOS
Pin Compatible with AD7510DI Series

GENERAL DESCRIPTION

The AD7590DI, AD7591DI and AD7592DI are a family of protected (latch-proof) dielectrically isolated CMOS switches featuring overvoltage protection up to $\pm 25V$ above the power supplies. Microprocessor interfacing is facilitated by the provision of on-chip data latches.

The AD7590DI and AD7591DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the switch control logic is inverted. The AD7592DI has two independent SPDT switches packaged in a 14-pin DIP.

FUNCTIONAL BLOCK DIAGRAMS

CONTROL LOGIC (WR HELD LOW)

AD7590DI: Switch "ON" for Address "HIGH"

AD7591DI: Switch "ON" for Address "LOW"

AD7592DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

AD7590DI/AD7591DI/AD7592DI—SPECIFICATIONS ($V_{DD} = 15V, V_{SS} = -15V$ unless otherwise noted)

Parameter	Model	$T_A = +25^\circ\text{C}$ (K, B, T)		$T_A =$ 0 to +70°C(K) -25°C to +85°C(B)		$-55^\circ\text{C to } +125^\circ\text{C(T)}$		Units	Test Conditions/Comments
ANALOG SWITCH									
Analog Signal Range	All	± 10	± 10	± 10				Volts	
R_{ON}^1	All	60	60	120	150			Ω typ	$-10V \leq V_S \leq +10V, I_{DS} = 1mA;$
	All	90	120					Ω max	Test Circuit 1
R_{ON} Match ²	All	2						Ω typ	$V_S = 0, I_{DS} = 1mA$
R_{ON} Match Drift ²	All	0.01						$\Omega/^\circ\text{C}$ typ	$V_S = 0, I_{DS} = 1mA$
I_D OFF ¹	AD7590DI	0.5				200		nA typ	Test Circuit 2
	AD7591DI	5	50					nA max	
I_S OFF ¹	All	0.5				200		nA typ	Test Circuits 2 & 4
		5	50					nA max	
$J_D(I_S)$ ON ¹	All	0.5				200		nA typ	Test Circuit 3
		5	50					nA max	
I_{OUT}^1	AD7592DI	1	100			400		nA typ	Test Circuit 4
		10						nA max	
$C_S(C_D)$ OFF ³	All	10						pF typ	
$C_S(C_D)$ ON ³	All	30						pF typ	
$C_{DS}(C_{S-OUT})$	All	1						pF typ	
$C_{DD}(C_{SS})^3$	All	0.5						pF typ	
C_{OUT}^3	AD7592DI	40						pF typ	
DIGITAL CONTROL									
V_{INL}^1	All	0.8	0.8	0.8				V max	
V_{INH}^1	All	2.4	2.4	2.4				V min	
C_{IN}^3	All	7	7	7				pF typ	
I_{INL} or $I_{INH}^{1,4}$	All	1	1	1				μA max	$V_{IN} = 0$ or V_{DD}
DYNAMIC CHARACTERISTICS									
t_{ON}^2	AD7590DI	250	380	380	500	500		ns max	Test Circuit 5
	AD7591DI	400	500	500				ns max	
t_{OFF}^2	AD7590DI	400	500	500	500	500		ns max	Test Circuit 5
	AD7591DI	250	380	380	500	500		ns max	
$t_{TRANSITION}^2$	AD7592DI	350	450	450	500	500		ns max	Test Circuit 6
Write Pulse-Width (t_{WR}) ²	All	250	300	300	400	400		ns min	See Figure 1
Address Setup Time (t_{AS}) ²	All	300	300	300	400	400		ns min	See Figure 1
Address Hold Time (t_{AH}) ²	All	20	30	30	40	40		ns min	See Figure 1
Off Isolation ³ (Analog Input to Analog Output) All		-85						dB typ	$A, \overline{WR} = 0.8V; V_S = 10V$ (Pk-Pk); $f = 1kHz, R_L = 10k\Omega$
Crosstalk ³ (Digital Input to Analog Output) All		5						mV peak, typ	$R_L = 1M\Omega, C_L = 15pF;$ $V_{INH} = 3V, V_{INL} = 0V;$ $t_{RISE} = t_{FALL} = 20ns;$ \overline{WR} held HIGH
Q_{INJ}^3 (Charge Injection)	All	55						pC typ	Test Circuit 7
POWER SUPPLY									
I_{DD}^1	All	1	1.5	2				mA max	Digital Inputs = V_{INL} or V_{INH}
I_{SS}^1	All	1	1	1				mA max	

NOTES

¹100% tested.

²Guaranteed, not production tested.

³Typical values for information only, not subject to test.

⁴Inputs are MOS gates typical current less than 10nA.

Specifications subject to change without notice.

TIMING AND CONTROL SEQUENCE

Figure 1 shows the timing sequence for latching the switch address inputs. The latches are level sensitive and, therefore, while \overline{WR} is held low the latches are transparent and the switches respond to the address inputs. The digital inputs are latched on the rising edge of \overline{WR} .

NOTE: All digital input signals rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 20ns$.

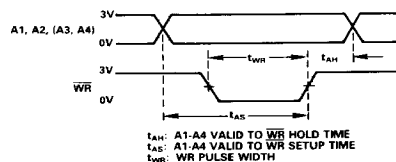


Figure 1. Timing and Control Sequence

AD7590DI/AD7591DI/AD7592DI

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V _{DD} to GND	+17V
V _{SS} to GND	-17V
Overvoltage at V _D (V _S), One Switch Only (1sec surge)	V _{DD} +25V or V _{SS} -25V
(Continuous)	V _{DD} +20V or V _{SS} -20V or 20mA, Whichever Occurs First
Switch Current (I _{DS} , Continuous)	50mA
Switch Current (I _{DS} , Surge)	150mA
1ms Duration, 10% Duty Cycle	150mA
Digital Input Voltage Range	-0.3V to V _{DD} +0.3V
Power Dissipation (Any Package)	450mW
Up to +75°C	450mW
Derates above +75°C by	6mW/°C
Storage Temperature	-65°C to +150°C
Operating Temperature	
Plastic (KN Versions)	0 to +70°C
Cerdip (BQ Versions)	-25°C to +85°C
Cerdip (TQ Versions)	-55°C to +125°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model ¹	Temperature Range	Package Option ²
AD7590DIKN	0°C to +70°C	N-16
AD7590DIKP	0°C to +70°C	P-20A
AD7590DIBQ	-25°C to +85°C	Q-16
AD7590DITQ	-55°C to +125°C	Q-16
AD7591DIKN	0°C to +70°C	N-16
AD7591DIKP	0°C to +70°C	P-20A
AD7591DIBQ	-25°C to +85°C	Q-16
AD7591DITQ	-55°C to +125°C	Q-16
AD7592DIKN	0°C to +70°C	N-14
AD7592DIKP	0°C to +70°C	P-20A
AD7592DIBQ	-25°C to +85°C	Q-14
AD7592DITQ	-55°C to +125°C	Q-14

NOTES

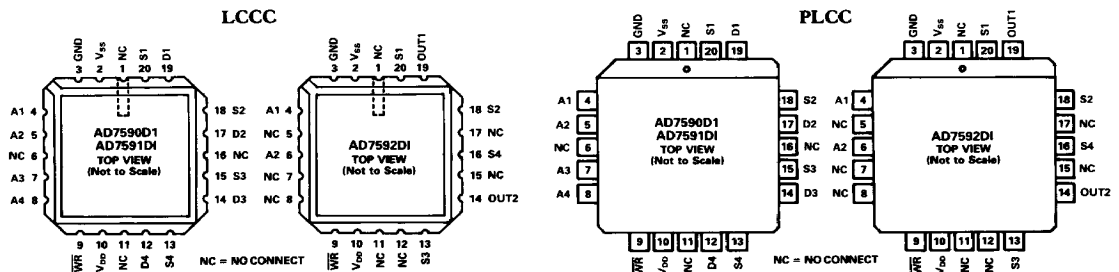
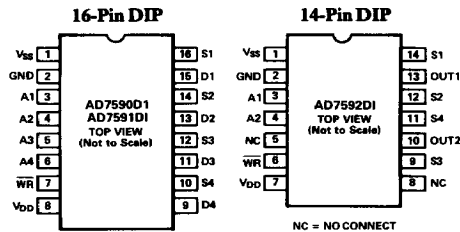
¹To order MIL-STD-883C, Class B processed parts, add /883B to part number. Refer to the Analog Devices Military Products Databook (1990) for military data sheet.

²N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier Q = Cerdip. For Hermetic Surface Mount package, contact your local sales office. For outline information see Package Information section.

5



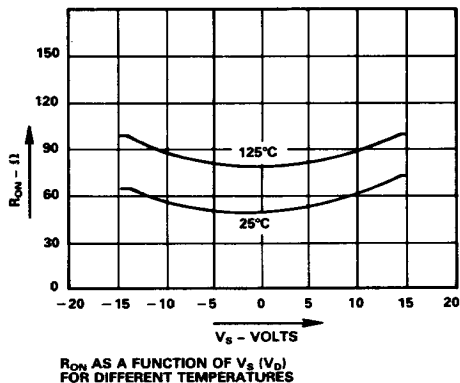
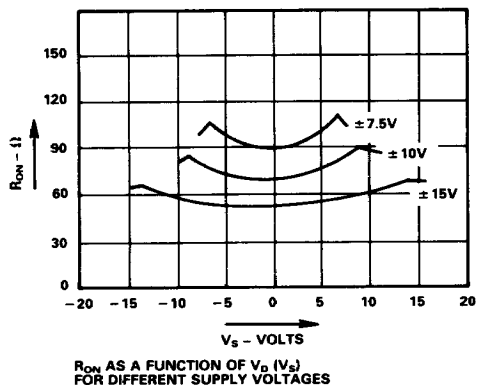
PIN CONFIGURATIONS



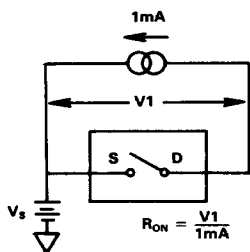
REV. A

CMOS SWITCHES & MULTIPLEXERS 5-27

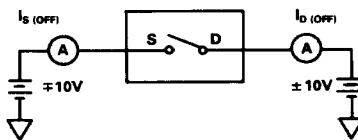
Typical Performance Characteristics and Test Circuits



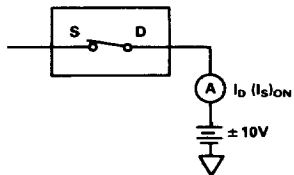
TEST CIRCUIT 1



TEST CIRCUIT 2
(AD7590DI, AD7591DI)

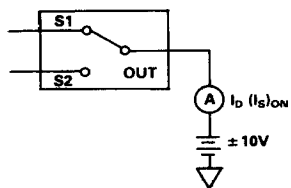
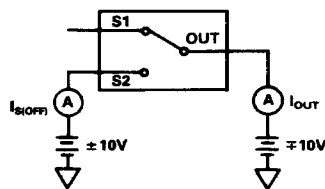


TEST CIRCUIT 3



a. AD7590DI, AD7591DI

TEST CIRCUIT 4
(AD7592DI ONLY)



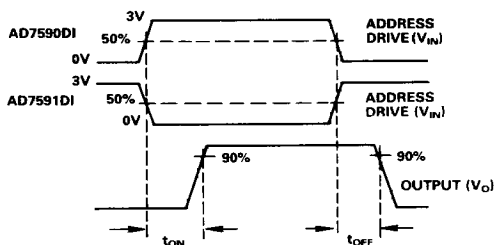
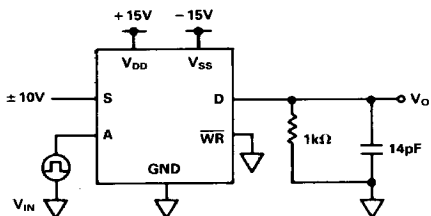
b. AD7592

AD7590DI/AD7591DI/AD7592DI

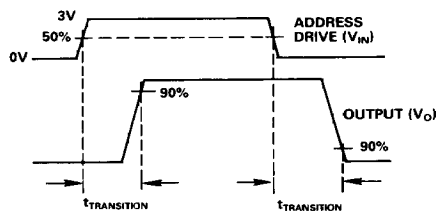
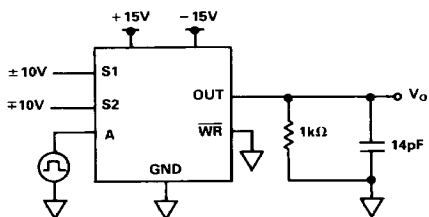
Typical Switching Characteristics and Test Circuits

Note: All digital input signal rise and fall times measured from 10% to 90% of 3V. $t_r = t_f = 20\text{ns}$.

TEST CIRCUIT 5
SWITCHING TIME OF AD7590DI AND AD7591DI, t_{ON} , t_{OFF}



TEST CIRCUIT 6
SWITCHING TIME OF AD7592DI, $t_{TRANSITION}$



TEST CIRCUIT 7
CHARGE INJECTION

